

1 1. A method of fabricating a semiconductor device,
2 comprising:

3 depositing a first material on a surface, the
4 first material having a first etch rate;

5 forming a trench through the first material and
6 into the surface; and

7 depositing a trench filler material in the trench,
8 the trench filler material having an etch rate that is
9 substantially similar to or less than the first etch rate.

1 2. The method of claim 1, including removing the
2 first material.

1 3. The method of claim 2, including depositing at
2 least a portion of a sacrificial layer of a second material
3 on the trench filler material and the surface.

1 4. The method of claim 3, including annealing the
2 sacrificial layer.

1 5. The method of claim 4, wherein said annealing step
2 forms a thermally grown portion of said sacrificial layer.

1 6. The method of claim 3, including implanting a
2 dopant into the substrate through the sacrificial layer and
3 removing the sacrificial layer.

1 7. The method of claim 3, including forming a
2 sacrificial layer by deposition and thermal growth.

1 8. The method of claim 2, including depositing a
2 sacrificial layer of a second material on the trench filler
3 material, the second material having an etch rate
4 substantially similar to or less than the etch rate of the
5 trench filler material.

1 9. The method of claim 8, including annealing the
2 sacrificial layer.

1 10. The method of claim 1 wherein the first material
2 includes an oxide.

1 11. The method of claim 10 wherein the first material
2 includes silicon dioxide deposited from
3 tetraethylorthosilicate or a silane and oxygen system.

1 12. The method of claim 10 wherein the first material
2 is deposited by chemical vapor deposition.

1 13. The method of claim 9 wherein the trench filler
2 material includes an oxide.

1 14. The method of claim 13 wherein the trench filler
2 material is deposited by chemical vapor deposition.

1 15. The method of claim 8 wherein the first material,
2 the second material and the trench filler material are
3 silicon dioxide.

1 16. A method of providing a sacrificial layer on a
2 semiconductor structure having a trench structure filled
3 with a trench filler material, comprising:

4 depositing a layer of a first material over the
5 trench filler material and the structure; and
6 annealing the layer.

1 17. The method of claim 16 wherein the etch rates of
2 said trench filler material and said first material are
3 substantially similar.

1 18. The method of claim 17 wherein both the first
2 material and the trench filler material include silicon
3 dioxide.

1 19. The method of claim 18 wherein the silicon dioxide
2 is deposited from tetraethylorthosilicate or a silane and
3 oxygen system.

1 20. The method of claim 18 wherein the silicon dioxide
2 is deposited by chemical vapor deposition.

1 21. The method of claim 16, including implanting a
2 dopant into the substrate through the sacrificial layer.

1 22. The method of claim 16, including growing an oxide
2 layer.

1 23. The method of claim 22, wherein said oxide layer
2 is grown during said annealing step.

1 24. The method of claim 22, wherein said oxide layer
2 is grown before said first layer is deposited.

1 25. The method of claim 22, wherein said oxide layer
2 is grown after said first layer is deposited.

S ubc17 26. A semiconductor structure, comprising:
1 a support;
2 a first material deposited on said support, the
3 first material having a first etch rate;
4 a trench formed through the first material and
5 into the support; and
6 a trench filler material deposited in the trench,
7 the trench filler material having an etch rate that is
8 substantially similar to or less than the first etch rate.

1 27. The semiconductor device of claim 26, wherein the
2 first material includes silicon dioxide deposited from
3 tetraethylorthosilicate or a silane and oxygen system.

1 28. The semiconductor device of claim 26, wherein the
2 first material includes silicon dioxide deposited by
3 chemical vapor deposition.

1 29. The semiconductor device of claim 26, wherein the
2 trench filler material includes silicon dioxide deposited
3 from tetraethylorthosilicate or a silane and oxygen system. ✓

1 30. The semiconductor device of claim 26, wherein the
2 trench filler material includes silicon dioxide deposited by
3 chemical vapor deposition.

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1 31. A semiconductor structure having a trench,
2 comprising:
3 a trench filler material that fills the trench;
4 and
5 at least a portion of a second material deposited
6 on the trench filler material and the structure,
7 wherein the second material is annealed.

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1 32. The semiconductor device of claim 31, wherein the
2 etch rate of the second material is substantially similar to
3 or less than the etch rate of the first material.

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1 33. The semiconductor device of claim 32, wherein both
2 the second material and the trench filler material include
3 silicon dioxide.

1 34. The semiconductor device of claim 31, wherein a
2 portion of said second material is thermally grown.

1 35. A method of forming trench isolation structures in
2 semiconductor devices comprising:
3 forming a layer on a semiconductor member;
4 forming a trench through said layer and into said
5 member;
6 filling said trench with a trench filling
7 material; and
8 etching said trench filling material and removing
9 said layer without forming grooves in the remaining trench
10 filling material.

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